IN THE CLAIMS

The following is a complete listing of the claims:

1. (currently amended) A programmable logic device, comprising:

a routing structure configured to provide logical inputs;

a plurality of logic blocks, each logic block including a programmable AND array operable to provide a plurality of product terms from a plurality of the logical inputs provided by the routing structure, the plurality of product terms being arranged the same for each logic block; wherein a first one of the logic blocks forms a receiver logic block and a second one of the logic blocks forms a feeder logic block, the receiver logic block having an AND gate for each product term, each AND gate being operable to receive its product term and the corresponding product term in the feeder logic block, each corresponding product term being cascaded from the feeder logic block over a dedicated lead, and wherein each AND gate is operable to receive its product term and the corresponding product term in the feeder logic block through the operation of programmable fuses.

2. (cancelled)

3. (original) The programmable logic device of claim 1, wherein each logic block further comprises a plurality of macrocells, each macrocell coupling to a cluster OR gate operable to sum a cluster of the cascaded product terms from the AND gates such that each macrocell may register the sum of cascaded product terms from its cluster OR gate.

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4. (original) The programmable logic device of claim 1, wherein the receiver logic block further comprises a plurality of macrocells, each macrocell coupling to an N-input cluster OR gate operable to sum a plurality of N of the cascaded product terms from the AND gates such that each macrocell may register the sum of cascaded product terms from its N-input cluster OR gate, the macrocells being arranged from a first macrocell to a last macrocell such that the first macrocell's N-input cluster OR gate may sum the first through the Nth cascaded product term, and so on.

5. (original) The programmable logic device of claim 1, wherein the receiver logic block further comprises:

a plurality of multiplexers corresponding on a one-to-one basis with the plurality of AND gates, wherein each multiplexer is operable to select between its AND gate's product term input and the cascaded product term output to provide a selected signal, and wherein each logic block includes a plurality of macrocells, each macrocell coupling to a cluster OR gate operable to sum a cluster of the selected signals such that each macrocell may register a sum of cascaded product terms or a sum of product terms, whereby the inter-logic-block width cascading provided by the plurality of AND gates may be bypassed.

6. (original) The programmable logic device of claim 5, wherein each AND gate is operable to receive its product term and the corresponding product term in the feeder logic block through the operation of programmable fuses.

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7. (original) The programmable logic device of claim 6, wherein, for each AND gate, the programmable fuses are arranged in a group and can be activated only as a group.

8. (currently amended) A programmable logic device, comprising:

a routing structure configured to provide logical inputs;

a plurality of logic blocks arranged from a first logic block to a last logic block, wherein each logic block includes a programmable AND array operable to provide a plurality of product terms from a plurality of the logical inputs provided by the routing structure, the plurality of product terms being arranged the same for each logic block, the first logic block being configured to cascade its products terms to the second logic block, the second logic block being configured to form the product of its product terms with the cascaded product terms from the first logic block and cascade the products to the third logic block, and so on such that the last logic block is configured to form the product of its product terms with the cascaded products from the next-to-the last logic block, and wherein the cascaded product terms and products propagate on dedicated paths separate from the routing structure, and wherein each logic block further comprises a plurality of macrocells, each macrocell coupling to a cluster OR gate operable to sum a cluster of the cascaded product terms such that each macrocell may register the sum of cascaded product terms from its cluster OR gate.

9. (original) The programmable logic device of claim 8, wherein each logic block is configured to form products of its product terms using logic circuitry.

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10. (original) The programmable logic device of claim 9, wherein the logic circuitry comprises an AND gate for each product term.

11. (original) The programmable logic device of claim 8, wherein the last logic block is a fourth logic block.

12. (currently amended) A programmable logic device, comprising:

a plurality of logic blocks each operable to provide a plurality of product terms selected from a plurality of logical inputs provided by a routing structure, wherein the plurality of product terms is arranged the same for each logic block and wherein the size of the plurality of logical inputs is the same for each logic block; and

means for cascading product terms, wherein the means is configured to form the product of the product terms from a first one of the logic blocks with the corresponding product terms selected from one or more of the remaining logic blocks, and wherein for each logic block selected, the maximum-achievable input width for the product is increased by the plurality of logical inputs, and wherein each logic block further comprises a plurality of macrocells, each macrocell coupling to a cluster OR gate operable to sum a cluster of cascaded product terms such that each macrocell may register the sum of cascaded product terms from its cluster OR gate.

13. (original) The programmable logic device of claim 12, wherein the plurality of logical inputs is 68 inputs.

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14. (original) The programmable logic device of claim 12, wherein the plurality of logic blocks comprises four logic blocks.

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